

Application Serial No: 10/593,674

Responsive to the Office Action mailed on: November 25, 2008

### **REMARKS**

This Amendment is in response to the Office Action mailed on November 25, 2008. No new matter is added. Claims 1-3 are amended. The amendments to claim 1 are supported, for example, in Figure 2 of the present application. Claim 2 is amended to track the amendments to claim 1. The amendments to claim 3 are supported, for example, in Figures 2 and 4 of the present application. Claims 6-12 are cancelled without prejudice or disclaimer. Claims 13-17 are new. Claims 13 and 14 are supported, for example, in Figures 2 and 4 of the present application. Claims 15-17 are supported, for example, in Figures 9 and 10 of the present application. Claims 1-5 and 13-17 are pending.

### **§102 Rejections:**

Claims 1-3 are rejected as being anticipated by Tsukada (US Publication No. 2005/0266615). This rejection is traversed.

Claim 1 is directed to a chip resistor that requires, among other features, a chip-like resistor element including a bottom surface, an upper surface opposite to the bottom surface, two end surfaces and two side surfaces, a plurality of electrodes spaced from each other on the bottom surface of the resistor element, and an insulator between the electrodes. Claim 1 also requires that at least one of the electrodes includes a non-overlapping portion held in direct contact with the bottom surface of the resistor element and an overlapping portion laminated over the insulator at a position away from the bottom surface of the resistor element, the overlapping portion including a flat mounting surface extending in parallel to the bottom surface of the resistor element.

Tsukada does not disclose or suggest these features. The rejection interprets the resistive element 1, the electrodes 3 and the insulation layer 4 of Tsukada as the chip-like resistor element, the electrodes and the insulator of claim 1, respectively. However, as shown in Figure 3 of Tsukada, each of the electrodes 3 overlaps only the corresponding edge of the insulation film 4 and therefore does not disclose an overlapping portion that includes a flat mounting surface extending in parallel to the bottom surface of the resistive element 1, as required by the overlapping portion of claim 1. Thus, nowhere does Tsukada disclose or suggest that at least one of the electrodes includes an

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overlapping portion laminated over the insulator at a position away from the bottom surface of the resistor element, the overlapping portion including a flat mounting surface extending in parallel to the bottom surface of the resistor element, as required by the electrodes, the insulator and the resistor element of claim 1. For at least these reasons claim 1 is not disclosed by Tsukada and should be allowed. Claims 2 and 3 depend from claim 1 and should be allowed for at least the same reasons.

§103 Rejections:

Claims 4 and 5 are rejected as being unpatentable over Tsukada in view of JP '009 (JP No. 2000-114009). This rejection is traversed. Claims 4 and 5 depend from claim 1 and should be allowed for at least the same reasons described above. Applicants do not concede the correctness of this rejection.

New Claims:

In order to expedite the prosecution of this matter, the following is noted with respect to new claims 13-17 as they relate to Tsukada and JP '009.

Claims 13 and 14 depend from claim 1 and should be allowed for at least the same reasons described above.

Claim 15 is directed to chip resistor that requires, among other features, a chip-like resistor element including a bottom surface, an upper surface opposite to the bottom surface, two end surfaces and two side surfaces, a plurality of electrodes spaced from each other on the bottom surface of the resistor element, and an insulator between the electrodes. Claim 15 also requires that the insulator includes a first portion between the electrodes, and a second portion formed integral with the first portion and laminated over each of the electrodes at a position away from the bottom surface of the resistor element.

Neither Tsukada nor JP '009 either alone or in combination teach or suggest these features. In particular, nowhere does either Tsukada or JP '009 teach or suggest an insulator that includes a first portion between the electrodes, and a second portion formed integral with the first portion and laminated over each of the electrodes at a position away from the bottom surface of the resistor element. Tsukada merely teaches that the electrodes 3 abuts or at most overlaps a corresponding edge of the insulation film 4, but

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does not contemplate the insulation layer 4 having a portion laminated over each of the electrodes 3 at a position away from the bottom surface of the resistive element 15. JP '009 is merely provided in the present Office Action as teaching a soldering layer that covers the end surface of a resistor element and electrodes and also does not teach or suggest an insulator that includes a first portion between the electrodes, and a second portion formed integral with the first portion and laminated over each of the electrodes at a position away from the bottom surface of the resistor element, as required by claim 15. For at least these reasons claim 15 is not suggested by Tsukada and JP '009, either alone or in combination, and should be allowed. Claims 16 and 17 depend from claim 15 and should be allowed for at least the same reasons.

Conclusion:

Applicants respectfully assert that claims 1-5 and 13-17 are in condition for allowance. If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Applicants' primary attorney-of record, James A. Larson (Reg. No. 40,443), at (612) 455-3805.




Dated: April 27, 2009

Respectfully submitted,

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